UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,149,881 B2
APPLICATION NO. : 10/804865
DATED : December 12, 2006
INVENTOR(S) : Sailesh Kottapalli et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 4, line 36: "No-op"
 should be --non-execution--

Column 4, line 37: "No-op"
 should be --non-execution--

Column 4, line 38: "process NOP instructions of said plurality of instructions"
 should be --process instructions to take no action for an instruction
   cycle--

Column 4, line 47-48: "No-op port coupled to said dispersal logic, said No-op port
   to process NOP instructions of said plurality of instructions"
 should be --a non-execution port coupled to said dispersal logic, said
   non-execution port to process instructions to take no action for
   an instruction cycle--

Column 4, line 61: "claim 6"
 should be --claim 5--

Column 4, line 65: "claim 7"
 should be --claim 6--

Column 4, line 67: "No-op"
 should be --non-execution--

Column 5, line 1: "claim 8"
 should be --claim 7--

Column 5, line 3: "No-op"
 should be --non-execution--

Column 5, line 6: "No-op"
 should be --non-execution--

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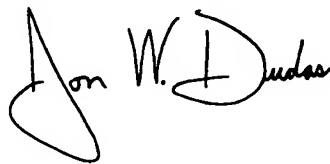INVENTOR(S)   : Sailesh Kottapalli et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 5,   lines 7-9: "determining if an instruction is a NOP instruction; and
dispersing said NOP instruction for execution by a No-op port"
should be --determining if an instruction is an instruction to take no action for an instruction cycle; and
dispersing said instruction to take no action for an instruction cycle for execution by a non-execution port--

Signed and Sealed this

Twenty-fifth Day of March, 2008

JON W. DUDAS
Director of the United States Patent and Trademark Office